IN THE DRAWINGS

No objection to the drawings, as filed on June 15, 2005, was indicated by the Examiner. Unless an indication is provided by the Office to the contrary, Applicants assume the drawings to be acceptable.

REMARKS

Claims 1-26 remain pending in this application.

The cross-reference issues cited by the Examiner has been addressed. The cross-references to the partially related application has been updated with relevant status.

The Examiner objected to claims 1-11 and 24 based upon mental process. Applicants respectfully disagree. Applicants have amended claim 24 to address the Examiner's concerns. Applicants respectfully asserts that claims 1-11 recite a novel process that is statutory subject matter. Applicants respectfully asserts that contrary to Examiner's assertion (in paragraph 2 of the Final Office Action dated September 30, 2005), 35 U.S.C. 101 does not require that a process or method must recite "a computer implemented method" to be statutory subject matter. The requirements under 35 U.S.C. 101 calls for a novel, non-obvious process, which is the subject matter of claims 1-11 and 24. Therefore claims 1-11 and 24 contain allowable subject matter, and thereby are allowable.

The Examiner rejected claims 4-5, 8-11, 15 and 20-21 under 35 U.S.C. 112, second paragraph, as being indefinite. Amendments have been made to claims 4, 8, 15, and 20 to address the Examiner's concerns. In light of the amendments, all indefiniteness issues cited the Examiner have been addressed. Therefore, claims 4, 8, 15, and 20 are allowable. Further, claims 5, 9-11, and 21, which are dependent from the rejected claims are also allowable for at least the same reasons. Accordingly, claims 4-5, 8-11, 15 and 20-21 are allowable.

The Examiner rejected claims 1-4, 6-20, 22, 23, 25 and 26 under 35 U.S. 102(e) as being anticipated by U.S. Patent No. 6,745,307 ***(McKee)***. Applicants respectfully traverse this rejection.

In the Final Office Action dated September 30, 2005, the Examiner argued that ***McKee*** teaches performing a virtual address based memory access. The Examiner cites, among other passages, the translation of the virtual memory address 502 to a physical memory address 508 disclosed on column 7, lines 35 onwards. However, this disclosure is related to performing the translation using a virtual memory table 514. The use of the virtual memory table as described below, does not anticipate the use of a secondary table, as well as a virtual memory table called for by claims of the present invention. The portion cited by the Examiner relates to performing the physical virtual memory address to physical memory address translation entirely by a processor without operating system intervention. Further, the usage of the TLB and the virtual page address of ***McKee*** does not teach, disclose, or suggest performing a virtual address memory access using a secondary table and at least one virtual memory table as called for by claim 1 of the present invention.

McKee simply does not teach, disclose, or suggest all of the elements of claim 1 of the present invention. For example, the virtual memory access called for by claim 1 of the present invention calls for performing a virtual address based memory access that is based on a secondary table and at least one virtual memory table. The Examiner asserted that this element is anticipated by the usage of the TLB and the virtual page address 505 of ***McKee.*** The Examiner asserted that this disclosure anticipated the use of the secondary and of virtual memory table of claim 4, as well as claim 1. Applicants respectfully disagree. Applicants respectfully assert that

the use of the secondary table as well as the virtual memory table is not anticipated by the TLB and the virtual page address 505 of ***McKee***.

The TLB is a translation look-aside buffer. The TLB contains data that is actually written by an operating system. For example, ***McKee*** discloses that the virtual page table entry 602 contains additional fields from which information required for a TLB entry can be retrieved. See col. 8, line 66 col. 9, line 1. ***McKee*** discloses that if the operating system successfully translates the virtual memory address into a physical memory address, that translation, both as a virtual page table entry and as a TLB entry, is inserted into the TLB. See col. 9, lines 1-4. This disclosure makes it clear that data is entered into the TLB as a result of translating virtual memory address into physical memory address, and not used to perform a virtual address based memory access. In other words, the virtual address based memory access is not performed using the TLB and the virtual page table 602, contrary to the Examiner's assertions. In fact, the above cited passage in ***McKee*** makes it abundantly clear that the prior art discloses that memory access is performed prior to writing data into the TLB *i.e.*, the virtual memory address being translated into a physical memory address. Subsequently, that information is then entered into the TLB. Therefore, it is erroneous to argue that the virtual address memory access in ***McKee*** is performed using two entities, such as the TLB and the virtual address table. Hence, the disclosure of the memory access in ***McKee*** is in stark contrast with the virtual address based memory access called for by claim 1 of the present invention, which calls for using a secondary table and a virtual memory table. Therefore, Applicants respectfully assert that the usage by ***McKee*** of the TLB and the virtual page table do not equate, anticipate or make obvious the element of the virtual address

memory based access called for by claim 1, which calls for using a secondary table and a virtual table access.

In fact, ***McKee*** simply does not disclose a secondary table. The Examiner's usage of the TLB is erroneous since data is written into the TLB, wherein virtual memory access called for by claim 1 of present invention uses information in the secondary table as well as a virtual memory table. In other words, ***McKee*** does not anticipate the subject matter of virtual address memory access using a secondary table and a virtual table access. Therefore, claim 1 of the present invention is not taught, disclosed or suggested by ***McKee***. Accordingly, claim 1 of the present invention is allowable.

Similarly, claim 8 calls for a method that provides for the memory access using a virtual address, wherein the access includes utilizing a secondary table, as well as at least one virtual memory table. Additionally, claims 12, 13 and 17 call for various apparatus and/or computer systems that called for performing a memory access using a virtual address, wherein the access includes utilizing a secondary table as well as at least one virtual memory table. Therefore, claims 8, 12, 13 and 17 are also not taught disclosures suggested by ***McKee*** for at least the reasons cited above.

Independent claims 1, 8, 12, 13, and 17 (all as amended) are allowable for at least the reasons cited above. Additionally, dependent claims 2-7, 9-11, 14-16, and 18-23, which respectively depend from claims 1, 8, 12, 13, and 17, are also allowable for at least the reasons cited above.

Applicants acknowledge and appreciate that the Examiner asserted that claims 5 and 21 contained allowable subject matter. Additionally, Previously presented claims 24 comprises subject matter that the Examiner has asserted is allowable and, therefore, is also allowable for at least the reasons cited herein.

Reconsideration of the present application is respectfully requested. In light of the arguments presented above, Applicants respectfully assert that claims 1-26 are allowable. In light of the arguments presented above, a Notice of Allowance is respectfully solicited.

If for any reason the Examiner finds the application other than in condition for allowance, **the Examiner is requested to call the undersigned attorney at the Houston, Texas telephone number (713) 934-4069** to discuss the steps necessary for placing the application in condition for allowance.

Respectfully submitted,

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